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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/550,282	04/14/2000	Sung-Il Park	1607-0211P	9574

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EXAMINER
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ART UNIT	PAPER NUMBER
2871	

DATE MAILED: 11/20/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/550,282	PARK ET AL.	
	Examiner	Art Unit	
	Mike Qi	2871	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 October 2002* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 6,172,728 (Hiraishi) in view of Applicant admitted prior art and US 6,100,954 (Kim et al).

Claims 1, 15 and 22, Hiraishi discloses (col.5, line 4 – col.7, line 41;Figs.1-2) a liquid crystal display device comprising:

(concerning claims 1 and 15)

- gate line (2) formed on a transparent substrate (10), the gate line (2) having gate electrodes (12) connected thereto (the gate electrode '12' protruding from the gate line '2');
- source line (3) (data lines) crossing the gate line (2) and formed on the transparent substrate (10);
- gate insulating layer (7) electrically insulating the data line (3) and the gate line (2);
- thin film transistor (TFT) (1) formed at an intersection of the gate line (2) and the data line (3), and connected to the gate line (2) and the data line (3);

- insulating layer (8) (functions as a passivation layer) formed over the TFT (1);
- pixel electrode (4) formed on the surface of the insulating layer (8) (functions as a passivation layer) to act as a light shielding layer, and the pixel electrode (4) proving a gap space (between the two pixel electrodes) over the data line (3) so as not to shield light therefrom (see Figs.1-2), therefore, the data line (3) having no light shielding layer formed thereover;
- a low-reflective film preferably made of chromium oxide on the source lines (3) (data line) to enhance the display quality.

(concerning claim 22)

- gate electrode (12) protruding from the gate line (2) is formed on a transparent substrate (10), i.e., forming a gate line and gate electrode connected thereto on a transparent substrate;
- forming gate insulating film (7) over the gate line (2) and the data line (3) (see Fig.2);
- forming a semiconductor layer (15) over the gate electrode (12);
- forming a date line (3) crossing the gate line (2), a source electrode (13) connected to the data line (3) and on a first portion (such as left portion) of the semiconductor layer (15), and a drain electrode (14) on second portion (such as right portion) of the semiconductor layer (15);

- forming interlayer insulating film (8) (functions as a passivation layer) having a contact hole (9a) exposing the drain electrode (14) over the transparent substrate (10);
- forming pixel electrode (4) on the interlayer insulating film (8) (functions as a passivation layer) to act as a light shielding layer, and the pixel electrode (4) proving a gap space (between the two pixel electrodes) over the data line (3) so as not to shield light therefrom (see Figs.1-2), therefore, the data line (3) having no light shielding layer formed thereover, and the pixel electrode (4) is connected to the drain electrode (14) via the contact hole (9a);
- a low-reflective film preferably made of chromium oxide on the source line (3) (data line) to enhance the display quality.

Although the structure disclosed by Hiraishi is not exactly same as the application claimed, but all the limitations claimed in the claims 1, 15 and 22 are covered by Hiraishi except for the limitation of the pixel electrode is not over the gate electrode.

However, Applicant admitted prior art discloses (Fig.1) that the pixel electrode (30) is not over the gate electrode (14), and that was known in the prior art as applicant admitted. Kim also discloses (Fig.1) that the pixel electrode (31) is not over the gate electrode (13), and such AMLCD structure is a conventional structure.

Especially, for the limitation of the low reflective layer formed on the data line, Hiraishi indicates (col.6, lines 34-37) that by providing a low-reflective film preferably

made of chromium oxide (CrOx) on the gate lines (2) and the source lines (3) (data line), the display quality is enhanced.

Therefore, it would have been obvious to those skilled in the art at the time the invention was made to form a low reflective layer on at least a portion of the date line and the pixel electrode is not over the gate electrode as claimed in claims 1, 15 and 22 for enhancing the display quality.

Claims 2 and 16, Hiraishi indicated (col.6, lines 34-37) that by providing a low-reflective film preferably made of chromium oxide (CrOx) on the gate lines (2) and the source lines (3) (data line), the display quality is enhanced. Therefore, it would have been obvious to those skilled in the art at the time the invention was made to form a low reflective layer on at least a portion of the gate line as claimed in claims 2, 13 and 23 for enhancing the display quality.

Claims 3-4, 6-8,10, 17-19 and 21, Hiraishi discloses (col.6, lines 13 – 37; Fig.2) that the thin film transistor (TFT1) includes a gate electrode (12), a source electrode (13) and a drain electrode (14), and a gate electrode (12) protruding from the gate line (2) (see Fig.2, same as the source/drain electrodes, a source electrode (13) protruding from the data line (3)), so that the gate electrode (12) is connected to the gate line (2) and the source electrode is connected to the date line (3). Hiraishi indicates (col.6, lines 34-37) that by providing a low-reflective film preferably made of chromium oxide (CrOx) on the gate lines (2) and the source lines (3) (data line), the display quality is enhanced. Therefore, forming a low reflective layer on the gate electrode and on the source/drain

electrodes as claimed in claims 3-4, 6-8, 10, 17-19 and 21 to enhance the display quality would have been at least an obvious variation.

Claims 11, Hiraishi discloses (col.5, lines 8 –11; col.6, lines 43-44; Fig.2) that an interlayer insulating film (8) (functions as a passivation layer) is formed entirely over the TFT (1), the gate line (2) and the source line (3) (data line), and a pixel electrode (4) is formed on the interlayer insulating film (8) (functions as a passivation layer) and connecting with the drain electrode (14) via contact hole (9a) in the interlayer insulating film (8) (functions as a passivation layer). Hiraishi indicated (col.6, lines 34-37) providing a low-reflective film on the gate lines (2) and the data lines (3), so that the interlayer insulating film (8) (functions as a passivation layer) is also formed over the low-reflective film.

Claims 12-13, 23-24, Hiraishi discloses (col.5, lines 56-57; Fig.1) that the pixel electrode (4) is formed over a portion of the data line (3) and over a portion of the gate line (2).

Claims 14 and 25, Hiraishi discloses (col.7, lines 13 – 24) that color film is provided on the counter substrate (20) (color filter substrate) is desired; and a liquid crystal material (30) sealed between the color filter substrate (20) and the transparent substrate (10).

Claims 5, 9 and 20, Applicant admitted prior art discloses (page 4, lines 2-3 of the specification) that the reflectivity of CrOx is about 3%, and that is the property of a material. Using CrOx as the low-reflective layer, the material CrOx must have such reflectivity, and that would have been at least obvious.

Response to Arguments

3. Applicant's arguments filed on Oct.28, 2002 have been fully considered but they are not persuasive.

Applicant's **only** arguments are as follows:

1) Hiraishi does not disclose a pixel electrode formed on the surface of the passivation layer, but not over the gate electrode to act as a light shielding layer therefore, the pixels electrode proving a gap space over the data line so as not to shield light there from as claimed in claim1, 15 and 22.

2) The device of Hiraishi provides a light shielding means (pixel electrode 4 and light-shielding layer 23) for both the gate line and the data line in spite of the low-reflective layer. Hence, the low-reflective layer for the light shielding layer of Hiraishi provides no hint to substitute the low-reflective layer for the light shielding layers used in the device.

Examiner's responses to Applicant's **only** arguments are as follows:

1) Hiraishi discloses (col.5, line 4 – col.7, line 41;Figs.1-2) a liquid crystal display device comprising pixel electrode (4) formed on the surface of the insulating layer (8) (functions as a passivation layer) to act as a light shielding layer, and the pixel electrode (4) proving a gap space (between the two pixel electrodes) over the data line (3) so as not to shield light therefrom (see Figs.1-2). Applicant admitted prior art discloses (Fig.1) that the pixel electrode (30) is not over the gate electrode (14), and that was known in the prior art as applicant admitted. Kim also discloses (Fig.1) that the pixel electrode

(31) is not over the gate electrode (13), and such AMLCD structure is a conventional structure.

2) The device of Hiraishi provides a light shielding means (pixel electrode 4 and light-shielding layer 23) for both the gate line and the data line in spite of the low-reflective layer which is a second example of the invention as shown in Fig.4. However, Hiraishi also discloses a first example of the invention as shown in Figs.1-2 in which the pixel electrode acts as a light shielding layer and providing a low-reflective film (CrOx) on the gate line and the source line (data line) to enhance the display quality.

Conclusion

4. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

6. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Mike Qi
November 14, 2002